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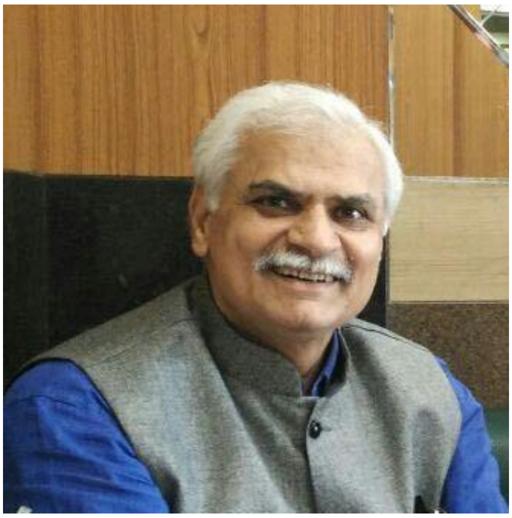
MESSAGE AND NOTE THROUGH DESK

[A]. Mentor - Prof. (Dr). R.K. Khandal



Prof. Dr. R. K. Khandal

Brief Profile:

a. Prof. Dr. R.K. Khandal Is the President, R&D and Business Development at India Glycols Limited, a well renowned and one of its kind companies in the world manufacturing Surfactants from sugarcane molasses. Former Vice Chancellor, Uttar Pradesh Technical University, Lucknow, a Fellow of the Royal Society of Chemistry, London

b. Unanimously elected President of WAITRO (World Association of Industrial & Tech. Organizations), a UN body, 2010-2012 and 2012-2014

c. Expert member of High level Committees of Govt. of India:

   i. Ministry of Science and Technology
   ii. Ministry of Child and Women Welfare
   iii. Ministry of Food Processing Industries
   iv. Recruitment and Appraisal committees of CSIR, DRDO etc.

d. Guided 30 PhD's from 10 Universities. 15 International Patents published 118 research papers in peer reviewed journals, five books and two edited.

e. He has received several awards; prestigious ones include:
   i. INSME (International award for innovation);
   ii. R.N. Bangur Memorial award for novel technologies;
   iii. R.G. Deshpande award for popularizing Radiation processing technology;

iv. U.P. Ratna Award, 2014 for Transforming Technical Education in U.P.
v. Rajasthan Samman Award, 2015 from Rajasthan Associations;
vi. Meri Dilli award, 2010 for improving the living standards of citizens of Delhi
vii. Srishti awards for green technologies, waste management etc.
viii. Amity Academic Excellence award for pioneering research and academics
ix. AMAR UJALA Excellence Award for outstanding contribution to education
x. Life time achievement award by World Environment Congress in food preservation, safety, environment protection and renewable energy,
xi. Eminent Engineers Award by Institutions of Engineers, India
xii. Academic Excellence Award from Engineering Watch, India, in Singapore,

Growth Path:

a. Born on September 6, 1957, he started his career in 1982, as a **lecturer in Indian School of Mines, Dhanbad** at a very young age of less than 25 years.

b. In 1985, joined as a **Group leader in a UNIDO project of Govt. of India.** Post-Doctoral research` ~ 1 year in England and 2 years in France.

c. On return from France in 1991, joined as **Manager, ICI Specialty chemicals**, an MNC and worked for developing Technologies for specialty chemicals.

d. In 1993, joined **India Glycols Limited as General Manager.** Managed team of R&D and Production for 8 years to for new products for growth of the Company.

e. From 2001 to 2012, as the **Director, Shriram Institute, Delhi** established as a leader par excellence. Developed and established a self-sustainability model.

f. **DURING 2012 – 2015, AS THE** VICE CHANCELLOR OF UTTAR PRADESH TECHNICAL UNIVERSITY, **TRANSFORMED THE UNIVERSITY INTO AN INNOVATION UNIVERSITY**.

g. 2015 onwards, Prof. Khandal is, the **President, R&D and Business Development, India Glycols Limited,** a global supplier of Green performance chemicals

h. Prof. Khandal has been associated with leading private universities and institutions as a mentor

Virtues:

Prof. Khandal is a person of eminence with unique expertise and capabilities; a rare profile covering 360̊ research and innovation cycle in career: as an Academician and a Researcher (Govt. and Pvt.). He knows how to convert challenges into opportunities.

[B]. Patron - in - Chief: – Prof. S.K. Singh

He is serving the nation in the field of science & technology. He has completed his graduation degree in Engineering in Electronics & Communication Engineering, from B.I.T. Sindri, in 1986 and postgraduate in Business Management from X.L.R.I. Jamshedpur, in 2004.

He has 30 years of wide experience in applied Research, Product Development and Program Management besides developing algorithms and their implementation for real-time embedded applications for signal processing in technologies like Software Defined Radio, Digital Subscriber Line, Cable Modem, Meteor Burst Communications and Satellite communications.

Background Highlights:-

- 1986 - 1997, Defence Research & Development Organization (D.R.D.O.) as Scientist
- 1997 - 2006, As Engineering Manager / Program Manager in Multinationals like, Freescale Semiconductor, Ishoni Networks, General Electric Plessey etc.
- 2006 - 2008: Cofounded a Telecom Company Hertz Tele Networks Pvt. Ltd
- 2008 - 2010: Director: Genesis Futuristic Technology Ltd, Noida
- 2010 till date: Founded many organizations till date.
- He had Co-authored a paper on the issue of inter modulation products for D.S.P. based Modulators in 2nd International Symposium on "D.S.P. for Communication Systems" held at Adelaide in 2004. D.S.P. based Modulators: Problems and Solutions.

Message from the Patron - in - Chief's Desk:-

"SANKALAN:- The Journal of Science, Technology & Humanities" (I.S.S.N. Online:- 2455 - 3557) is a Journal started with a goal to publish innovative ideas which proposes value in creating technologies for tomorrow and solving problems of today right from concept to implementation.

This Journal will try to set an example for extending opportunities to scholars of different field to publish their papers with ethics and honesty. I wish a grand success to all the stakeholders of the Journal.

[C]. Executive Editor / Publisher: - Rahul Rai

He is working as Deputy Registrar at B.I.T. Mesra, Ranchi, Jharkhand. His areas of interest are Analytics, Marketing & Entrepreneurship. He is M.B.A with Distinction Marks from B.I.T.S., Pilani, Rajasthan and B.Tech with Distinction in IT and Management. He has 06 years of industrial experience in Analytics and Research industry.

Background Highlights:-

- Worked as Academic Associate in Department of Management, B.I.T.S., Pilani, Rajasthan
- Qualified All India Level :- U.G.C. National Eligibility Test – Junior Research Fellowship (U.G.C. – N.E.T – J.R.F.) in Management in the year 2013
- Diverse Experience in various domain like Banking, Retail, Media & Marketing
- Awarded Many Prizes and appreciations in the career in several fields till date
- Organized & Participated in several seminars and events till date

Note from the Publisher / Executive Editor's Desk:-

Wishing you all a great year ahead!!!

Firstly, I will pay my gratitude to Almighty, my parents and all well-wishers with whose blessings and support we are able to start this journal "**SANKALAN:-The Journal of Science, Technology and Humanities",** (I.S.S.N. Online: - 2455 - 3557) We have started this journal publication for publishing new findings on Science, Technology and Humanities.

I hope this initiative will bring great value for academicians, researchers, students and all those who are involved in Research & Development work. We do have a highly reputed pool of advisory board members from well renowned universities, who help us in keeping high benchmark for quality and originality of our publications. Hence, I am confident that our mission to be the leading Research Journal in field of science, technology and humanities will very soon become true.

I hope very soon Buxar- Land of Rishi Vishwamitra; will soon become educational hub of Bihar.

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[D]. Editor - in - Chief: - Rishabh Rai

He is the Editor in Chief of this Journal and working as a P.G.T. Physics and Mathematics in Carmel School, Churamanpur, Buxar, Bihar. His areas of interest are the domains of Electronics and Communication Engineering and Physics, Chemistry & Mathematics. He is M.Tech in V.L.S.I. Design specialization with Distinction Marks & B.Tech in Electronics & Telecommunication Engineering with Honours. Further, he is B.Ed. in Science stream with first class.

Background Highlights:-

- Awarded as the Best Innovative teacher of the year award by ISRO & NASA Delegates in the international level conference at Chandigarh, India on 29.09.2019
- Appreciated by the Govt. of India, Govt. of Bihar & Govt. of Jharkhand for the quality publication of the Journal – Sankalan: - The Journal of Science, Technology & Humanities (e - ISSN - 2455-3557), in the year 2016, 2017 & 2018d
- Appreciated by Kyutec University, Japan and Amazon, an online shopping company for the outstanding publication of the book " Be the change for best always and make difference"
- Earned the respective academic degrees in the career till date i.e. (Class X^{th} to M.Tech.) with Distinction / Honours in aggregate
- Published 20 Technical / Research / Review / Study Papers in several National / International Conferences and Journals till date
- Authored many books, chapters in various publications till date
- Awarded Honorarium & Appreciated for the Paper Publication by A.K.G.E.C. International Journal of Technology in 2016
- Academic Excellence Award, for the academic performance in M.Tech. – (2013 – 2015)
- Academic Excellence Award , for the aggregate performance in B.Tech (2009 - 2013)
- I.E.E.E. National Merit Award – 2013, for the best Paper Presentation in National Conference - E.T.E.A.T – 2013
- Project Selection in the Sixth Science Conclave – 2013, at I.I.I.T Allahabad
- Amul Vidya Bhushan Award – 2009, for the academic excellence & performance in A.I.S.S.C.E. – 2009
- Awarded many awards (Winner), recognitions, appreciations at International, National, State, District, College & School Level in various academics and cultural (Solo Singing, Writing Books, Journals etc.) events till date

Note from the Editor - in - Chief's Desk:-

Firstly, I am thankful to god and grateful to my venerated parents, and all those whose blessings and constant encouragement have helped me to complete this work, i.e. compilation and finalizing of the current issue of the Journal, "**SANKALAN:-The Journal of Science, Technology and Humanities", (I.S.S.N. Online: - 2455 - 3557)**. The papers must not be published, copied in parts or whole or accepted for publication anywhere else. For more information and ideas, one must visit the **"Quality & Plagiarism Check"** for such issues, as given in the website www.sankalan.org .

The entire article will must be double blind peer reviewed by our Advisory Board and will be thoroughly checked on the Plagiarism Software if selected, may be published by completing the copyright policies with the Journal. Lastly, I want to thank all the concerned authorities who are directly or indirectly related to our Journal, and must expect that their co-ordination and support are always valuable and required for us forever.

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OBJECTIVES:

- ❖ To develop and promote academic research activities on various contemporary techno-engineering issues and trends in management and humanities.
- ❖ To provide a platform to discuss the problems related to the technical as well as the managerial and research issues.

The most valuable and suggestive comments of all the readers are always awaited and welcomed in order to achieve the ultimate goal. We are looking forward for your contributions. All communications must be made only in electronic form e-mailed to:

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CONTENTS

CRISP VERSION OF THE SPECIAL ISSUE OF THE JOURNAL

SWITCHING TECHNOLOGY& ARCHITECTURE

Anil Agarawal, Academician

ABSTRACT—In this paper, the packet switching architecture with output queuing is used. Here the switch is internally non-blocking, but if packets destined to same outputs, output blocking will occur and (even if there are output queues) has a capacity of N*N^2. An exact model of the switch has been developed which can be used to determine the blocking performance of the switch and obtain both its throughput and packet loss characteristics. In this architecture, each line card is connected by a dedicated point to point link to the central switch fabric. Two structures can be classified as Centralized and Distributed. Buffer arrangements are also categorized into output queued and combined input- output queued switches and hardware complexity of OQ, VOQ are also discussed.

KEYWORDS- IQ Switches, OQ Switches, VOQ Switches, Switch Fabric.

I. INTRODUCTION

Over the past decade, data communication has been revolutionized by a radically new technology called Packet Switching. Packet switched routers need buffers during times of congestion. Buffer arrangements can be placed on inputs and outputs within the switch fabric. A major challenge connected to high-speed switching is related today to switch design that requires the best possible ease of implementation and good performance. The main functions of Switching are: (i) manage packet buffering while selecting packets to transmit each time to avoid contentions and cell loss. (ii) Routing packets from their incoming ports to their destination ports. To avoid contentions and cell loss, the incoming packets are stored in buffers. These buffers can be in inputs, in outputs, in inputs and outputs or shared by inputs and outputs. Although, a lot of existing switches use the shared buffers techniques. In OQ (Output Queue) strategy, all incoming cells at the input are allowed to arrive at the output port and they are served using FIFO (First in First Out) discipline. In this strategy, there is 100% throughput and there is an internal speedup of order of N (impractical for large N) [1]. An output buffered switch can be more complex than an input buffered switch because the switch fabric must operate at much higher speed to reduce the probability of cell loss.

The IQ (Input Queue) switch can transfer at most one packet from an input and at most one packet to an output in a slot. At the beginning of a slot, more than one HOL (Head of Line Blocking) cells from the input queues have the same destination, and then only one of them is switched and transmitted on the output link in the slot. These switches are easy to implement and throughput is limited to 58.6% under uniform traffic. The other HOL cells continue to be queued at their inputs. Thus, packets in an IQ switch can experience HOL blocking, in which a blocked HOL cell blocks the cells behind it in the input FIFO queue even though the destination ports of these other cells are free and are idling. One of the proposed solution for IQ switches which is VOQ. In this, the main aim is to overcome HOL blocking as there is no speed up requirement. It needs scheduling algorithms to resolve contention problems (i) complexity (ii) performance guarantee. Different scheduling algorithms for VOQ switches are considered most of them achieve 100% throughput under uniform traffic, but the throughput is reduced under non-uniform traffic.

II. LITERATURE SURVEY

J. Xian and Ch.-T. Lea et.al, 1991 [1] proposed a model in which they operated a technique called parallel iterative matching, which can quickly identify a set of conflict free cells for transmission in a time slot and a more flexible approach to high availability using multiple redundant paths between hosts. T. Anderson et.al, 1994 [2] used an N*N port input- queued switch with FIFO and according to him, the throughput is limited. J. H.J. Chao, C.H. Lam and E. Oki et.al, 1998 [3] proposed a model in which they found the optimal division between the input and output queues under different (space, time) combination and how that division shifted with the (space, time) implementation. N. McKeon, A. Mekkittikul, V. Anantharam and J. Walrand et.al, 1999 [4] proposed that bandwidth of optical fibers caused tremendous increase in speed of data transmission and a bit sliced crossbar fabric to switch packets at 10 Gb/s at inputs and outputs. H.J. Chao et.al, 2001 [5] proposed a model by designing a high capacity packet switch (e g. Multiple terabits/second) that: (1) supports individual line rates in excess of the speeds of available electronic memory and is capable of supporting the same qualities and service as an output-queued switch and from a more practical point of view, the arbitration should be separated from the output packet scheduling to keep the implementation and time complexities reasonable. Using speedup with input-output queuing is widely accepted as the most feasible solution to building large-scale switches and they also supported idea to emulate an input- output buffered switch with speedup as a purely output queued switch by specially scheduling cells from inputs to outputs such that each output is identical to the emulated purely output queued switch.

III. GENERAL ARCHITECTURE

Here the OQ switch, the fabric provides a dedicated point to point channel between each input and output. The figure-1 shows the switch architecture with output queuing is being used.

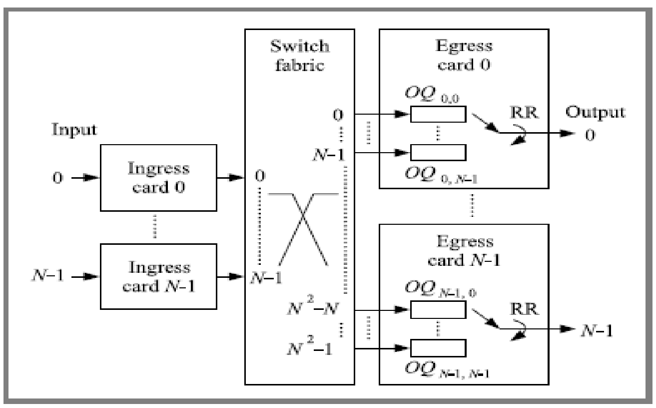

Figure-1. The Switch Architecture with Output Queuing.

In this figure, there are N input ports, N output ports and the switch fabric. They are implemented on separate ingress and egress card 0 to N-1. An input to ingress card is connected to switch fabric by one line, and this enables the switch to simultaneously transfer up to N packets to each output port. The figure-1 shows, at most N packets arrive during a time step, all packets are transferred to their respective outputs in the switching phase immediately following their arrival. At the output portside ($OQ_{j,i}$), each packet received from the input side stored in the output buffer receiving N packets from input port through the switch fabric. Therefore these packets can be simultaneously written to N-1 queues.

IV. SWITCHING FABRIC ARCHITECTURE

Now, we will consider the switching fabric architecture. The switch fabric has a capacity of $N*N^2$ and it uses a non-blocking switch fabric. There are configurations for using the switch fabric. It can reside on the backplane and can be connected directly with line cards or it can reside on a separate card attached to it connected through a mesh to all line cards. In central case, the switch fabric constitutes one module produced on several boards. They are simple on input and output and are arranged online cards. The centralized approach requires each input to contact a centralized scheduler at every arbitration cycle. With N ports, N request must be connected to line cards and processed by the arbiter each cycle.

This requires a high speed control path running at the line rate between every input and the central scheduler. In this case, the line cards are connected with the switch fabric by 2 lines, but the switch fabric will require more boards with buffer memories. The switch fabric of size $N*N^2$ can also be decentralized by putting each 1*N segment on each line card.

In centralized mode, the switch fabric is located on several ingress/ egress cards. A switch fabric on switch architecture of $N*N^2$ switch fabric, so that each row of crossbar switch fabric is placed on line cards [2]. The goal is to work on architecture that is scalable, both in terms of line speed as well as in terms of number of ports, at the same time flexible and reliable and can support different line cards. This requires a number of outputs from line cards. Each incoming and outgoing lines are connected to line cards and connections made between them act as buses and are broadcasted from inputs to all outputs. The function of address filter (AF filter) is in the given connection whether the packets in line cards are destined to output or not. The number of Address Filters is N*N size and it can operate with line speed.

When the traffic is uniformly distributed, servicing the maximum number of queues leads to 100% throughput. When it is non-uniform, some queues become longer than others. A good algorithm keeps the queue lengths matched, and service a large number of queues. The maximal weight algorithm in input queuing depends on the Fair Access Round Robin (FARR) and Longest Port First (LPF). For very low bandwidth systems, the choice of a shared Bus or shared- memory architecture is obvious. The result is a fully synchronous serial backplane that needs no phase reacquisition, after a switch reconfigures and therefore maximizes the usable bandwidth. Furthermore, some synchronous crossbar fabrics also have the arbitration and configuration control logic integrated in the switch.

V. BUFFER IMPLEMENTATIONS

The buffering operations consist in queuing the cells to transmit. The performances of the switch can be affected differently according to the way that is done. Different strategies are used depending on the physical site of the queues in both inputs and outputs, or are shared buffers. In this architecture, every output can receive simultaneously during the same cycle, N cells from the N inputs. Thus, the switch must be able to put in the same queue and during the same cycle, N cells from the N inputs. Packets from N queues in each output Port are readout using Round-Robin algorithm pointer denoted by RR, and modified in such a way, when all packets from the same position are already readout, the RR is set back to zero. In given figure-3, 3 time slots 1,2 and 3 from the switching fabric are shown. Packet Switching architecture uses a crossbar for interconnecting the cards on which ports reside. Despite the N^2 complexity, a cross-bar is actually the most popular switch core.

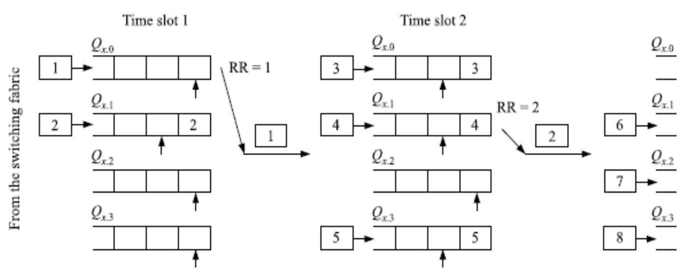

Figure-3. The Example of Buffer Operation with Separate Pointers.

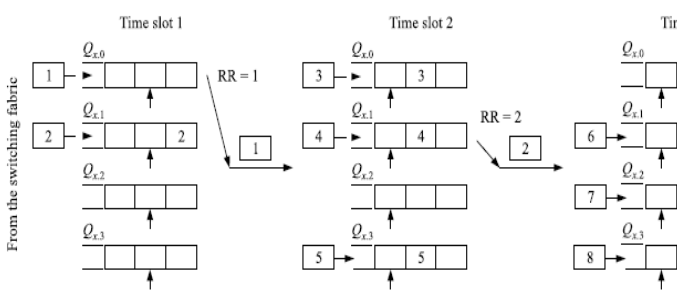

Figure-4. The Example of Buffer Operation with One Pointer.

The figure-3 shows the buffer operation with separate pointers shown by arrow signifies the state of the pointers in different time slots 1, 2 and 3. In time slot 1, the packets from the switching fabric 1 and 2 from inputs $Q_{x,\,0}$ and $Q_{X,\,1}$ is directed to output and RR is set to 1 i.e. (RR=1) and packet 2 from input 1 is stored in $Q_{X,\,1}$ [3]. In the next time slot 2, the packets from the switching fabric numbered as 3, 4 and 5 from inputs 0, 1 and 3 are directed to output and RR is set to 2 and packet 2 from $Q_{X,\,1}$ is sent out. In next time slot 3, the packets from the switching fabric numbered as 6,7 and 8 from inputs numbered as 1, 2 and 3 is immediately considered to output x and packet 7 is sent to the output. Packets 6 and 8 are stored in $Q_{X,\,1}$ and $Q_{X,\,3}$. In the other case, the figure-4 shows buffer operation with one pointer is assigned to all queues.

In time slot 1, the packets from the switching fabric 1 and 2 from inputs 0 and 1 are immediately sent to output x and Round Robin (RR) is set to zero.(Since HOL packet from $OQ_{X,0}$ has highest priority) as shown in figure-4, the packet 1 from input 0 is sent to output and packet 2 is stored in $Q_{x,1}$. In next time slot 2, the packets from switching fabric 3, 4 and 5 from inputs 0, 1 and 3 and the packet 2 from $Q_{x,\,1}$ is sent out. After this packet is sent out there is not other any packet in first memory cell. During the next time slot 3, packets from switching fabric 6, 7 and 8 from inputs numbered as 1, 2 and 3 and since RR is set to zero and packet 3 from $Q_{X,\,0}$ is sent immediately to the output. In next 3 time slots, the packets from switching fabric numbered as 4, 5 and 6 will be sent out to the output.

For the packet switching there is no special transport path established for a connection and variable length data packets carry information used by network nodes in making forwarding decisions. There is no signaling needed for connection setup. Forwarding tables in the network nodes are updated by routing protocols. The best effort service for all connections in conventional packet switched networks. The main problem of IQ (Input Queue) switching is HOL blocking, which can have a severe effect on throughput. It is well known that if each input maintains a single FIFO, then HOL blocking can limit the throughput to 58.6% [4]. One method is that has been proposed to reduce HOL blocking is to increase the speedup of a switch. A switch with a speed up of S (say) can remove upto S packets from each input and deliver upto S packets to each output within a time slot, where a time slot is the time between packet arrivals at input ports. Hence, an OQ switch has a speed up of N while an IQ switch has a speed up of 1. For values of S between 1 and N packets need to be buffered at the inputs before switching as well as at the outputs after switching.

We call this architecture a combined input and output queued (CIOQ) switch. In practice, we are not only interested in the throughput of a switch, but also in the latency of individual packets. Packets in an IQ switch not only contend for an output, they also contend for an entry into the switch fabric with packets that are destined for other outputs. This phenomenon is input contention. Each input can deliver only one packet into the fabric at a time; if it has packets for several free outputs, it must choose just one packet to deliver, holding other packets back. This place, a packet at the mercy of other packets destined for other outputs. This is in a stark contrast with output-queuing, where a packet is unaffected by packets destined for other outputs. CIOQ switches make no guarantees about the delay of an individual packet; instead they consider only average delay and throughput. While these switches are academically interesting, they give us the principle benefit of output queuing: the ability to control the delay of individual packets [5]. Rather than final values of speedup that work well on average, or with simplistic and unrealistic traffic models, we find the minimum speedup such that a CIOQ switch behaves identically to an OQ switch.

Although output buffers give the optimal delay-throughput performance, switches that use them are difficult to achieve. In output buffer method, every output can receive simultaneously during the same cycle, N cells from the N inputs. Thus, the switch must be able to put in the same queue and during one cycle, the N cells destined to the same output. The operation of setting in queue must therefore operate N times quickly than the rate of all arrivals (speed up). If, this solution is feasible in case of small capacity switches, it should not be possible for switches of big capacities (the N- times speed-up in the switch limits the scalability of this architecture). A major drawback of input buffer is related to queue managing while selecting cells to transmit at every cycle. The simplest way consists in storing the incoming cells in FIFO queues.

VI. COMPARISION TABLES

The differences between circuit switching, datagram packet switching and virtual circuit packet switching are shown in table 1 in which there is a dedicated path in circuit switching, there is no dedicated path in datagram packet switching and in virtual circuit packet switching, also there is no dedicated path. The differences between input queuing, output queuing and combined input and output queuing are shown in table 2 in which packets are stored at the input side in input queuing, packets are stored at the output side in output queuing and in combined input and output queuing packets are stored at both input and output sides. In input queuing switch speed is equal to line speed, in output queuing switch speed is equal to N times of line speed and in combined input and output queuing there is speedup between 1 and N. There is no overlapping in case of input queuing, in output queuing there is a redundant constraint and in combined input and output queuing there is shared memory switch. The hardware complexities of different buffer strategies are shown in table 3. The parameters like switch fabric speed in output queuing is N, in virtual output queuing it is 1, and in multiple output queuing is also 1 which is same as line speed. However, the switch fabric capacity in output queuing is N*N, in virtual output queuing is N*N and in MOQ architecture the capacity is $N*N^2$. Among the different buffer strategies the MOQ architecture is effective considering in high speed and high capacity switches. The memory speed in OQ architecture is N, in VOQ architecture, it is 1 and in MOQ architecture, it is also 1.

Table 1: - Difference between circuit switching, datagram packet and virtual circuit packet switching.

CIRCUIT SWITCHING	DATAGRAM PACKET SWITCHING	VIRTUAL CIRCUIT PACKET SWITCHING
Dedicated path	No dedicated path	No dedicated path
Call set up delay	Packet transmission delay	Call set up delay, packet transmission delay
No speed or code conversion	Speed or code conversion	Speed or code conversion
Fixed bandwidth	Dynamic bandwidth	Dynamic bandwidth
No overhead bit after call set up	Overhead bits in each packet	Overhead bits in each packet
Path established for entire connection	Route established for each packet	Route established for entire connection

Table 2:- Difference between input queuing, output queuing and combined input and output queuing.

INPUT QUEUEING	OUTPUT QUEUEING	COMBINED INPUT AND OUTPUT QUEUEING
Packets stored at the input	Packets stored at the output	Packets stored at both input and output
Switch speed is equal to line speed	Switch speed is equal to N* line speed	Speedup between 1 and N
Combination of packets can be transferred across a switch	Any N packets intended for an output can be transferred	Packets stored in the switch fabric, every output line reads when they transmit.

Input queued switch has additional rate constraints at the output	For output line stability these constraints will arise in output queued switches	For this queueing these constraints will arise at both input and output
Input queuing do not overlap	Redundant constraint	Shared memory switch
It operates on FIFO	There is 100% throughput	Values of speed up need to be buffered
HOL cells continue to be queued at their inputs	Can be more complex because it operates at a much higher speed	In this queuing there is minimum speed up

Table 3:- The hardware complexity of different buffer strategies.

Parameters	OQ	VOQ	MOQ
Switch fabric speed	N	1	1
Switch fabric hardware	N^2	N^2	N^2
Number of buffers	N	N^2	N^2
Memory speed	N	1	1
Number of schedulers	N	2N	N
Switch fabric capacity	N*N	N*N	$N*N^2$

The similar complexity is needed since each VOQ has to be connected with the scheduler to send request signal when it has a HOL packet. The OQ switches consist of N buffers and have to be N times faster than VOQ switches. Different switches of OQ switches are connected to input and output switches to their ingress and egress cards.

VII. CONCLUSION

In this paper, the packet switching architecture with output queuing has been used. The hardware complexity of OQ, compared to VOQ switches are also discussed and the considerations of OQ switches in different input-output queuing using buffer implementations are used in either separate chip or in the switch fabric architecture. The difference between different types of switching and difference between input queuing, output queuing and combined input and output queuing are also discussed.

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Spectroscopic Analysis of Electron Donor sites in Methylbutanoic acid

Prity Kumari, Academician

***Abstract*- Coumarins are oxygen containing heterocyclic compounds having unique photochemical and photo physical properties which depend on the electron donor atom or group present in it. (E)-2-(1-(4-hydroxy-2oxo-2H-Chromen-3yl) ethylideneamino)-3-methylbutanoic acid (HCMB) is coumarin derivative synthesized by condensation of 7-hydroxy-2-oxo-2H chromene-8-carbaldehyde and 2-amino-3-methylbutanoic acid and I.R., ^{1}H and ^{13}CNMR spectroscopic techniques exhibit the presence of electron donor atom which cause the fluorescence activity of synthesized molecule**

***Keywords* -** Coumarin derivatives, electron donor atoms

I. INTRODUCTION

Coumarin consists of a benzene ring fused together with a pyrone ring.

The pyrone ring also contains a double bond such that it extends the conjugate π system across the molecule. In Coumarin moiety an aromatic ring is contain six carbon atoms as ring -I and pyrone ring as ring-II. .

The various coumarin derivatives that bear an electron donor group are most commonly used for fluorescence applications. [1]

The unique photochemical and photo physical properties of coumarin derivatives make them useful in a variety of optical application such as in optical brighteners laser dyes, nonlinear optical chromophores, solar collector systems and organic light emitting diodes. [2-6]

The present paper deal with the synthesis of compound HCMB by the condensation of 7-hydroxy-2-oxo-2H chromene-8-carbaldehyde and 2-amino-3-methylbutanoic acid and identification of electron donor sites present in such compound by Electronic, I.R., ^{1}H and ^{13}CNMR spectroscopic techniques.

II. EXPERIMENTAL

i- Materials and Apparatus

All solvents were dried by standard methods. Starting materials were commercially available and were purchased from BDH chemicals Ltd.

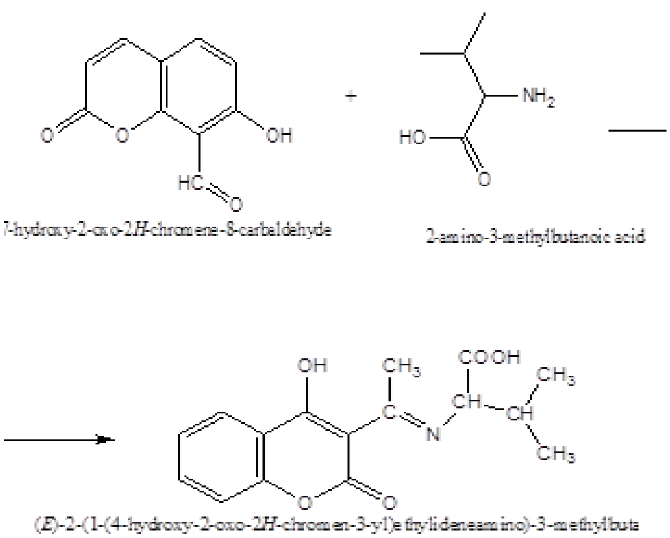
All solvents used are of HPLC or spectroscopic grade Product was purified by flash chromatography on silica gel (230–400 mesh, Merck) using Hexane: ethyl acetate (3:1) as eluent.

Melting points were taken on an Electro thermal X-4 apparatus. The IR spectra of synthesized compound is recorded in the range of 4000-400 cm^{-1}

This is done by using a Thermo Nicolet 320 FTIR spectrometer using KBr disc at room temperature ^{1}H NMR and ^{13}C NMR spectra were recorded on a Varian NMR system 400(400 MHz) with TMS as an internal standard. UV-Vis spectra were recorded with a 1-cm path quartz cell on a Shimadzu UV-2550.

ii. Synthesis of (E)-2-(1-(4-hydroxy-2oxo-2H-Chromen-3yl) ethylideneamino)-3-methylbutanoic acid (HCMB)-

The methanolic solution of 7-hydroxy-2-oxo-2H chromene-8-carbaldehyde (1.9 gm, 1mole) was added to the methanolic solution of 2-amino-3-methylbutanoic acid (1.17 gm, 1 mole) and the mixture was refluxed for 30 minute. After cooling the mixture, the solvent was evaporated and the residue was purified by column chromatography on silica gel (hexane-ethyl acetate, 4:1, volume ratio), yielding the product as yellow crystal. [7]



III. RESULTS AND DISCUSSION

i-Micro-Analysis:(E)-2-(1-(4-hydroxy-2oxo-2H-Chromen-3yl) ethylideneamino)-3-methylbutanoic acid (HCMB), $C_{16}H_{17}NO_5$, mol. wt 303, M.P. 125 °C, **C%=** 63.36,**H%**=5.65,**N%** =4.62,**O%**=26.37.

ii- UV-Vis Absorption Spectra

The electronic spectra of methanolic solution of HCMB observed at 497 nm, this band tentatively assigned to the $\pi \rightarrow \pi^*$ transition. [7-8] the electronic spectra of HCMB in various aqueous buffer solution are shown in Fig-1. The spectra show a small amount of bathochromic shift with increased pH.

Table:1

Solvent	Λmax	λex(nm)	E	ϕ
Methanol	457	475	520	1.05×10^{4}
Ethanol	468	475	515	1.25×10^{4}
Propanol	470	478	512	1.35×10^{4}
Butanol	465	485	510	1.30×10^{4}
Acetonitrile	479	465	525	1.75×10^{4}

ϕ, Quantum yield; ε, molar absorptivity L mol^{-1} cm^{-1}.

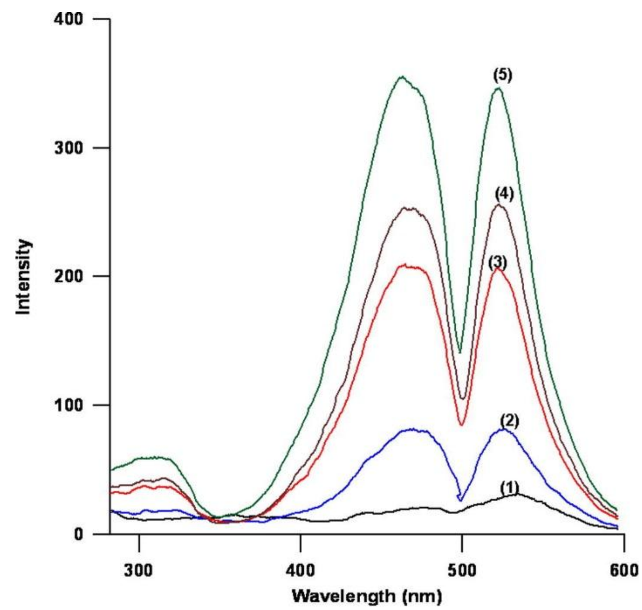


Fig 1

ii- I.R. Spectral studies

The IR spectra of HCMB show a broad band in region 3000-3200 cm^{-1} assigned to the stretching vibrations of –OH group. [9] the appearance of medium intensity band 1360-1350 cm^{-1} , 1230-1250 cm^{-1} suggested the presence of coumarin ring in compound. [10]The band appeared at 1660-1670 cm^{-1} & 1760-1690 cm^{-1}assigned to the lactone carbonyl moiety present in compound [11-12].

The appearance of medium intensity band 1360-1300 cm^{-1} suggested the presence of azomethine bond in HCMB while the presence of medium intensity band at 1615-1625 cm^{-1} and 1566-1570 cm^{-1} assigned to the existence of –COOH group in compound.[13]

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The IR spectral bands suggested the presence of following electron donor sites in HCMB

- Nitrogen atom of Azomethine bond (C=N bond)
- Oxygen atom of cyclic carbonyl group of coumarin ring
- -COOH group
- -OH group

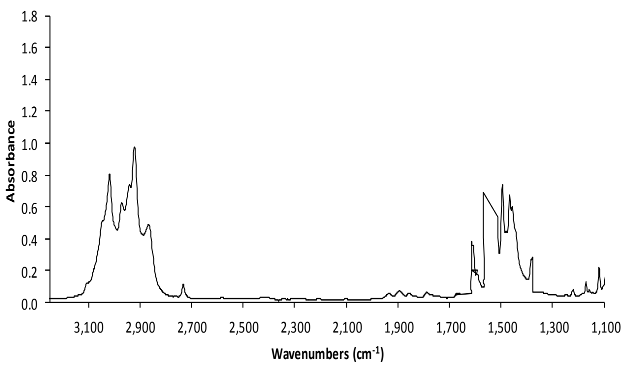

Fig 2- IR Spectra of HCMB

iii-H-NMR Spectral studies:- A multiple of proton signal appeared at δ =7.02-7.27 ppm assigned to the proton signal attached with C_5, C_6, C_7, C_8, C_9 and C_{10} atom of coumarin ring. [14] The appearance of singlet a δ =15 ppm suggested the presence of –OH group while another sharp singlet appearance at δ =11.0 ppm indicate the proton signal associated with –COOH group which can generate an electron donor site after deportonation**.** [15-17]

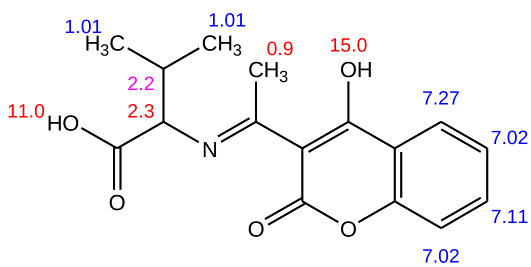

Fig 3 -^{1}HNMR chemical shift δ/ppm of HCMB

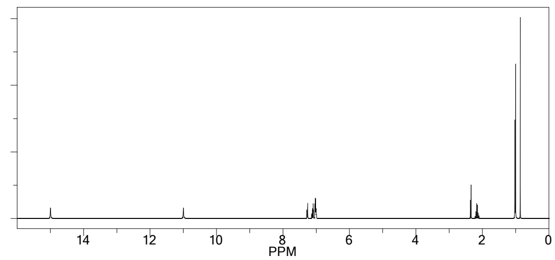

Fig 4 -^{1}HNMR Spectra of HCMB

v- ^{13}C NMR Spectral studies : the ^{13}CNMR spectra of HCMB show nine nonaromatic carbon signal at δ =159.5,165.3,126.8,125.5,128.4,121.5,150.2 & 117.5 ppm of C-2,C-3, C-4,C-5,C-6,C-7,C-8,C-9 and C-10 atom of 4-hydroxy coumarin ring.[18]. The carbon signal appeared at δ =159.5 ppm assigned to the C=O group carbon atom signal of coumarin ring. HCMB show a sharp signal at δ = 177 ppm assigned to the presence of azomethine bond. The sharp carbon signal appeared at δ = 177.5 ppm due to the presence of COOH group.[19-20].

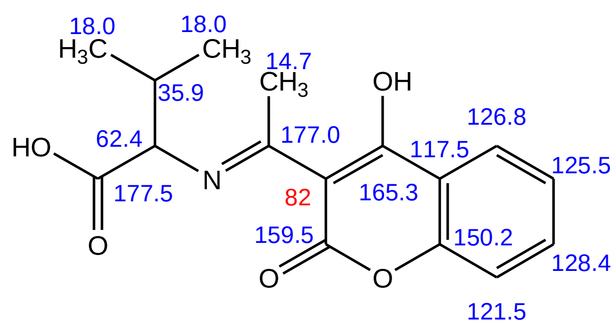

Fig 5 -^{13}C-NMR chemical shift δ/ppm of HCMB

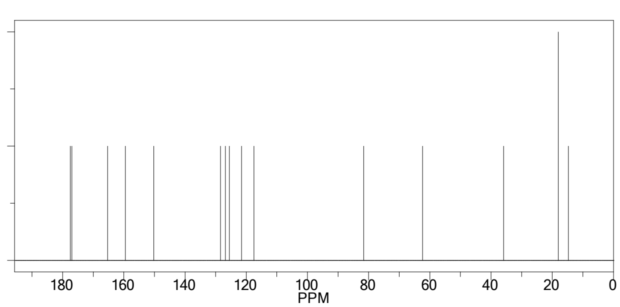

Fig 6- ^{13}CNMR Spectra of HCMB

IV. CONCLUSION

From the data of Electronic, I.R. and NMR spectral studies is observed that compound (E)-2-(1-(4-hydroxy-2oxo-2H-Chromen-3yl) ethylideneamino)-3-methylbutanoic acid (HCMB) have the following electron donor sites Nitrogen atom of Azomethine bond (C=N bond) Oxygen atom of cyclic carbonyl group of coumarin ring
-COOH group
-OH group

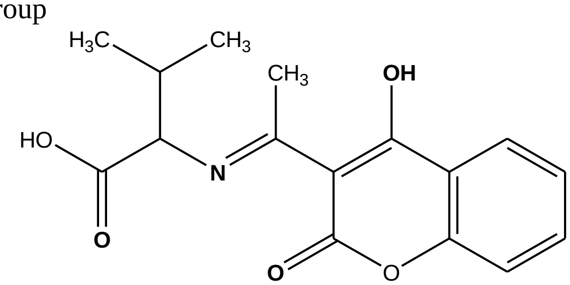

Fig 7

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